UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/090,840	03/06/2002	Toshihiro Saika	03500.016259	5736

5514 7590 03/09/2006

FITZPATRICK CELLA HARPER & SCINTO
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

EXAMINER	
LAM, HUNG H	

ART UNIT	PAPER NUMBER
2615	

DATE MAILED: 03/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/090,840	SAIKA, TOSHIHIRO	
	Examiner	Art Unit	
	Hung H. Lam	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/16/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☑ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/16/05 has been entered.

Response to Amendment

2. The amendments, filed on 12/16/05, have been entered and made of record. Claims 1-7 are pending.

Response to Arguments

3. Applicant's arguments filed 12/16/05 have been fully considered but they are not persuasive.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., a structure of a read-out pulse supplied by the scanning circuit to readout pixels while thinning the pixels out) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Further more, the language of the independent claim 1 only required a scanning circuit to supply "the first pulse to the pixel to be readout and a second pulse smaller than the first pulse to a pixel to be thinned out...first resolution is selected" Therefore, the claim cannot be interpreted as if the scanning circuit is supplying pulses to the pixels to be readout while thinning the pixels out.

The Applicants also argue that Terada fails to disclose or suggest the scanning circuit supplies different-width read-out signals to the pixels in accordance with a selected resolution in the manner recited in the amended claim 1. However, the Examiner respectfully disagrees. Terada teaches that by applying wider pulses ΦSR1-ΦSR7 to the odd and even line, interlace driving mode can be realized and thereby providing high resolution image (Figs. 2F, 2H, 2J, 2L, 3G, 3I, 3K; Col. 7, Ln. 38 – Col. 8, Ln. 21; Col. 9, Ln. 60-67; Col. 2, Ln. 5-6 wherein Terada further teaches that vertical selection pulses ΦSR1 to ΦSRn are used to drive pixels). In addition, Terada teaches narrower pulses ΦSR1-ΦSR7 in Figs. 2G, 2I, 2K, 3F, 3H, 3J causing complete odd/even line of pixels to be skipped in the non interlace mode and thereby providing low-resolution image (Col. 8, Ln. 1-43; Col. 9, Ln. 50-67; Col. 11, Ln. 15-28).

In view of the above, the Examiner believes that the broadest interpretation of the present claimed invention does in fact read on the cited reference for at least the reasons discussed above and as stated in the detail Office Action as follows.

Claim Objections

4. Claim 3 is objected to because of the following informalities: claim 1 requires a scanning circuit to supplies a first pulse to a pixel to be readout while the dependent claim 3

requires a signals which are read out by supplying the first pulse to said scanning circuit. For the purpose of examination, the examiner read claim 3 as "an apparatus comprising a signal processing circuit which performs image processing on the basis of signals which are read out by supplying the first pulse from said scanning circuit". Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 1-3 and 5-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Terada (US-6,124,888).

Regarding **claim 1**, Terada discloses an image processing apparatus comprising:

a sensor (Fig. 4) including a plurality of pixels each including a light receiving element (Fig. 1; diode D), and a scanning circuit (Fig. 4; horizontal 5/ vertical 7A scanning circuit) for reading out signals in time sequence from the plurality of pixels (Col. 9, Ln. 40-50; it is inherent that the horizontal 5/ vertical 7A scanning circuit read out image signals in time sequence); and

a drive circuit, which supplies pulses (Figs. 1 and 8: pulses ΦV1, ΦV2, ΦH1, ΦH2) for driving said scanning circuit (Fig. 7; Drive circuit 109; Col. 12, Ln. 11-18).

wherein said drive circuit (Fig. 7; 109) is so arranged to drive said scanning circuit (Col. 7, Ln. 28-42; Col. 12, Ln. 11-29) so that said scanning circuit supplies a first pulse to a pixel to be read out, when a first resolution is selected (Figs. 2F, 2H, 2J, 2L, 3G, 3I, 3K; Col. 7, Ln. 38 – Col. 8, Ln. 21; Terada teaches that by applying wider pulses ΦSR1-ΦSR7 to the odd and even

line, interlace driving mode can be realized and thereby providing high resolution image; Col. 9, Ln. 60-67; Col. 2, Ln. 5-6 wherein Terada further teaches that vertical selection pulses ΦSR1 to ΦSRn are used to drive pixels), and supplies the first pulse to the pixel to be read out (Col. 2, Ln. 5-6; Col. 7, Ln. 38 – Col. 8, Ln. 21; Col. 9, Ln. 60-67) and a second pulse smaller than the first pulse to a pixel to be thinned out, when a second resolution lower than the first resolution is selected (Col. 8, Ln. 1-43; Col. 9, Ln. 50-67; Col. 11, Ln. 15-28; Terada teaches narrower pulses ΦSR1-ΦSR7 in Figs. 2G, 2I, 2K, 3F, 3H, 3J causing complete odd/even line of pixels to be skipped in the non interlace mode and thereby providing low resolution image; it is also noticed that during the horizontal blanking period HBL the selection pulses ΦSRn in Figs. 2G, 2I, 2K, 3F, 3H, 3J, 3L are much narrower than the selection pulses ΦSRn in Figs. 2F, 2H, 2J, 2L, 3G, 3I, 3K).

Regarding **claim 2**, Terada discloses an apparatus wherein when the second resolution is selected, said drive circuit supplies the first pulse in every other pulse or in every plurality of pulses (Fig. 6A; Col. 8, Ln. 35-43; second resolution is selected and only odd lines ΦSR1 and ΦSR3 are selected for reading out; scanning circuit is provided with the wide pulse ΦV1 in every other narrow pulse {within HBL}; see Fig. 6A).

Regarding **claim 3**, Terada further discloses an apparatus comprising a signal processing circuit which performs image processing on the basis of signals which are read out by supplying the first pulse from said scanning circuit (Col. 9, Ln. 55-67; see Fig. 6A and 6D; the wider pulse in ΦSR1 is interpreted as the first pulse; it is noticed that when pulse ΦV1 and ΦSR1 are

high and then ΦV1 goes low at HBL while ΦSR1 is still high, a complete line of pixels is read out).

Regarding **claim 5**, Terada discloses an apparatus wherein each of said pixels has an amplifying device which amplifies a signal from the light receiving element, and which outputs the amplified signal (Fig. 4; Col. 8, Ln. 44-50; Terada teaches an amplification type solid-state imaging device; additionally, it is commonly known in the art that each pixel/ light receiving element is included with a transistor/ amplifier device for amplifying an image signal), a reset switch for resetting an input portion of said amplifying device (Col. 9, Ln. 1-10; it is inherent that the image sensor is included a reset switch in order for the reset voltage VRS to reset the input switch), and a selecting switch (Fig. 4, SW3) for selectively reading the signal from said amplifying device (Col. 9, Ln. 10-13), said selecting switch being supplied with a pulse from said scanning circuit (Col. 9, Ln. 10-15; Col. 9, Ln. 40-67).

Regarding **claim 6**, Terada further discloses an apparatus comprising a control circuit (Fig. 7; system controller 108) for switching between the first resolution and the second resolution (Col. 12, Ln. 11-29).

7. Claims 4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Terada.

Regarding **claim 4**, Terada discloses an apparatus as recited in the rejection of claim 2. However, Terada fails to explicitly disclose that the sensor is formed on the same semiconductor chip, and a plurality of said sensors are mounted on a mount board.

However, the examiner takes Official Notice that it is well known and expected in the art for forming image sensors on the same semiconductor chip and mounting sensors on a printed circuit board. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the image processing apparatus of Terada by forming the sensors on the same semiconductor chip and mounting them on the board in order to provide a wide dynamic range image sensor having a compact structure.

As Applicant has not traversed the old and well known statement set forth above, "the sensor is formed on the same semiconductor chip, and a plurality of said sensors are mounted on a mount board" is now taken as admitted prior art. See MPEP 2144.03(c).

Regarding **claim 7**, Terada discloses an apparatus as recited in claim 1. However, Terada fails to disclose a light source for irradiating light on said sensor, and a transport member for moving an original and said sensor relative to each other.

However, the examiner takes Official Notice that it is well known and expected in the art for providing a light to irradiate on a reading surface and a transport member for moving the sensor and an original relative to each other. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the image processing apparatus of Terada by having an irradiating light and a transport member in order to provide a scanner having adequate illumination.

As Applicant has not traversed the old and well known statement set forth above, "a light source for irradiating light on said sensor, and a transport member for moving an original and said sensor relative to each other" is now taken as admitted prior art. See MPEP 2144.03(c).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung H. Lam whose telephone number is 571-272-7367. The examiner can normally be reached on Monday - Friday 8AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, NGOC YEN VU can be reached on 571-272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HL
03/02/06

NGOC-YEN VU
SUPERVISORY PATENT EXAMINER